

(1)

LOGIC GATES

• VACUUM TUBES — ENIAC

• TRANSISTOR — INVENTED IN 1947
AT BELL LABS

— SWITCH — 2 STATES / ON
— OFF

• INTEGRATED CIRCUITS IC'S



GORDON MOORE — CO FOUNDER OF INTEL
MADE AN OBSERVATION KNOWN AS
MOORE'S LAW:

THE NO. OF TRANSISTORS YOU CAN FIT ON
A GIVEN AREA OF INTEGRATED CIRCUIT / CHIP
WILL TEND TO DOUBLE EVERY 18-24 MONTHS
APPROXIMATELY.

(2)

TRANSISTORS → GATES → CIRCUITS → CPL

GATES

AND

NOT (INVERTER)

XOR

OR

NAND

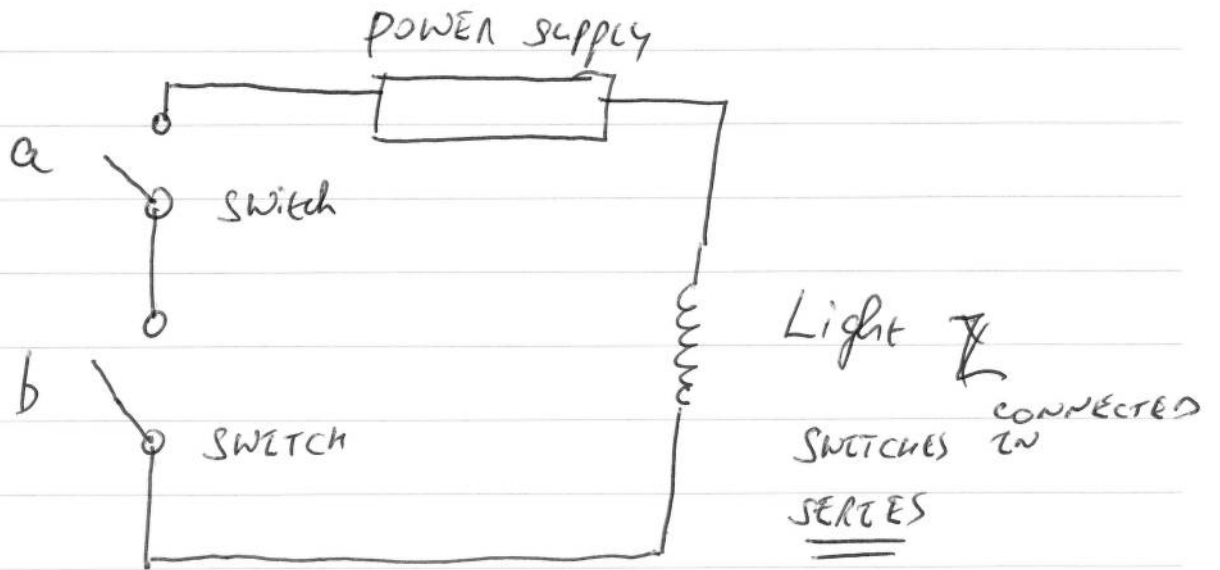
NOR

CIRCUITS

HALF-ADDER

FLIP FLOP

DECODER

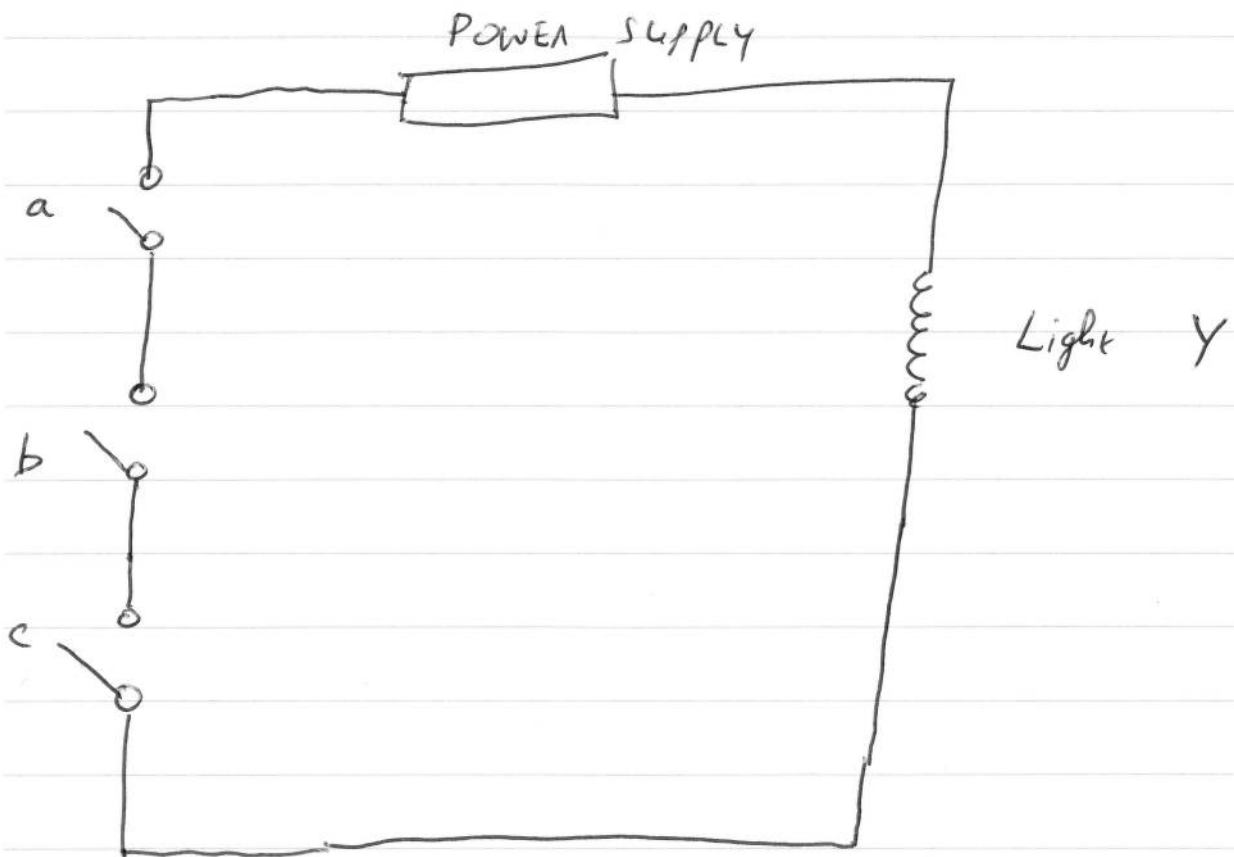


A	B	Y
OPEN	OPEN	OFF
OPEN	CLOSED	OFF
CLOSED	OPEN	OFF
CLOSED	CLOSED	ON

(3)

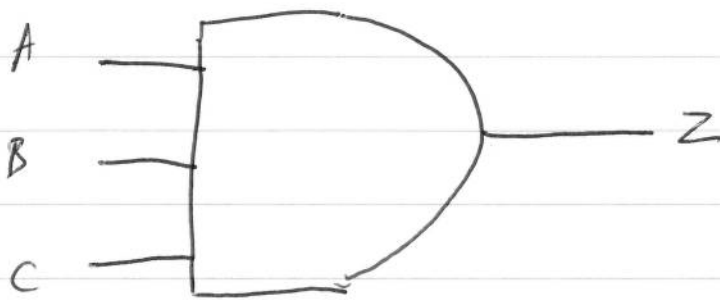
THE CIRCUIT PERFORMS A TWO INPUT AND
FUNCTION

A THREE INPUT VERSION COULD BE CONSTRUCTED
BY ADDING A 3RD SWITCH IN SERIES
WITH THE OTHER TWO



④

A	B	C	Z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1



④ ⑤

AND GATE

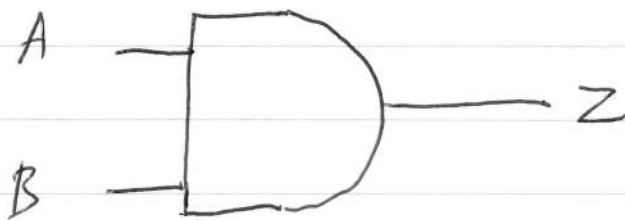
(TRUTH TABLE)

A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1

0 = OFF

1 = ON

WHEN BOTH A AND B ARE 1 THE OUTPUT Z IS 1.

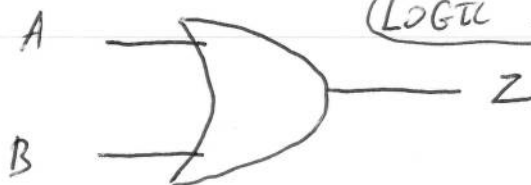


LOGIC SYMBOL

OR GATE

A	B	Z
0	0	0
0	1	1
1	0	1
1	1	1

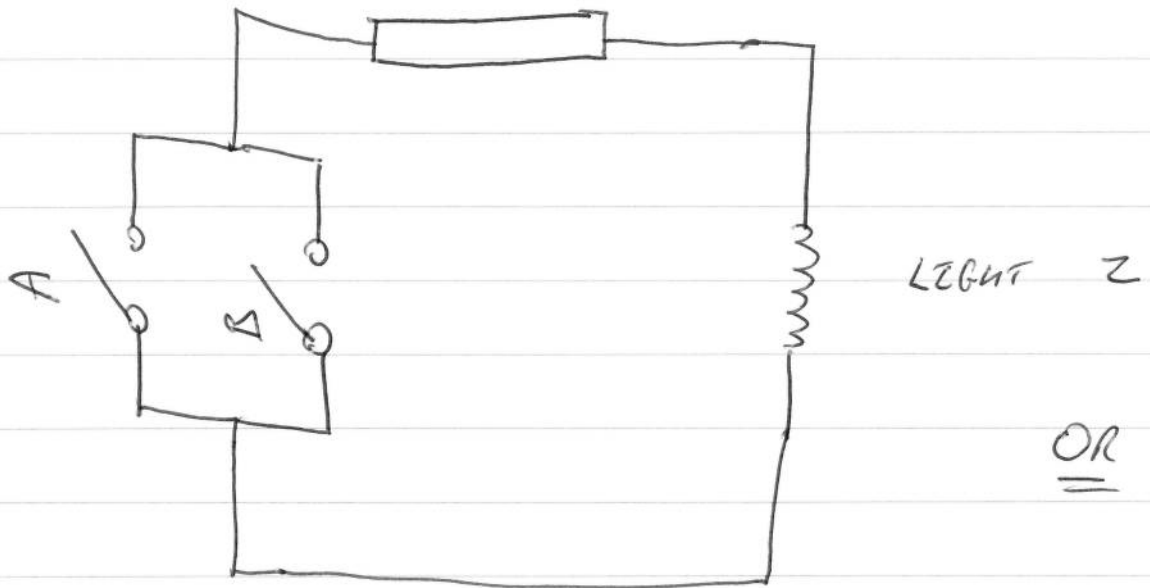
IF EITHER INPUT IS 1 (HIGH), THE OUTPUT IS 1.



LOGIC SYMBOL

5 6

POWER E.G. BATTERIES



OR

SWITCHES CONNECTED IN PARALLEL

(7)

NOT (INVERTER)

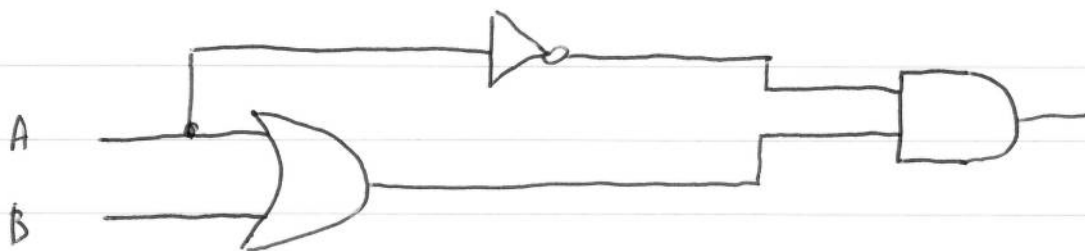


TRUTH TABLE

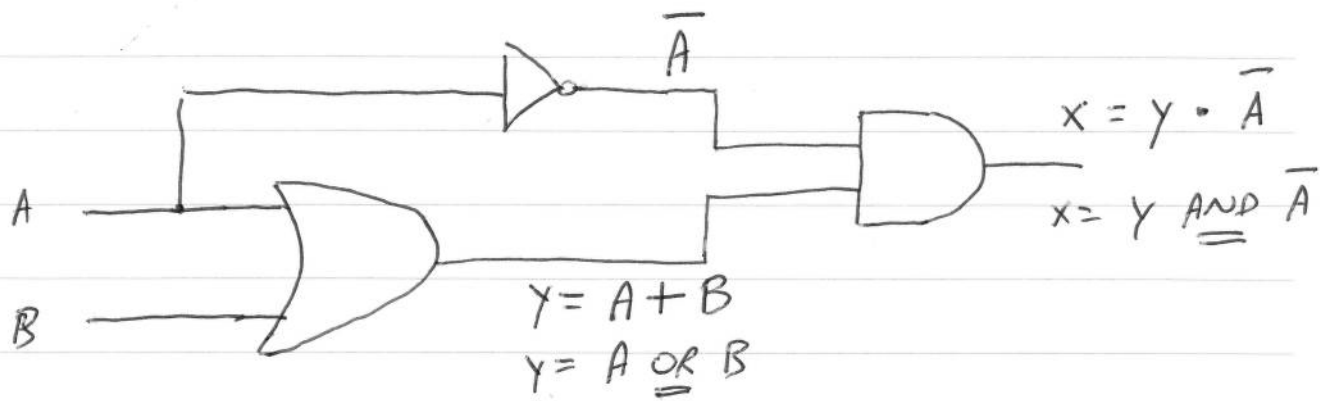
A	Z
0	1
1	0



(DL3) - EXAMPLE COMBINING GATES



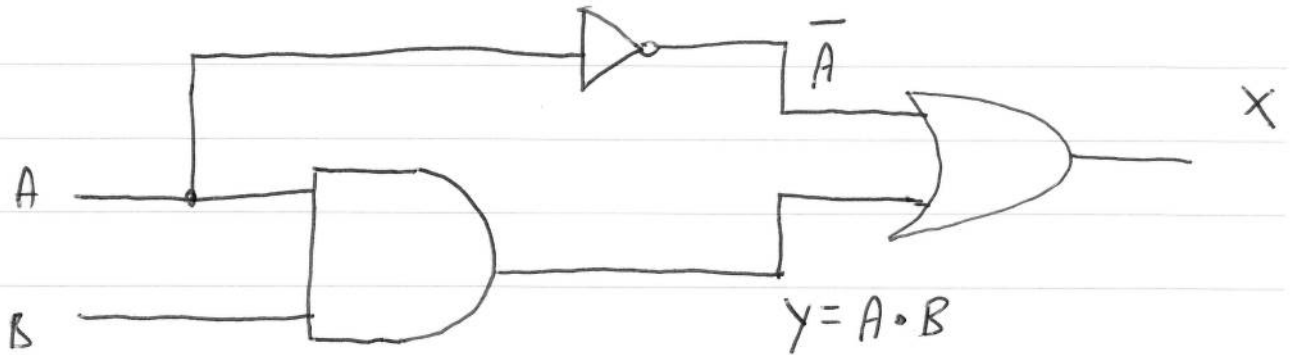
8



A	B	Y	\bar{A}	X
0	0	0	1	0
0	1	1	1	1
1	0	1	0	0
1	1	1	0	0

9

(DL.4)



A	B	Y	\bar{A}	X
0	0	0	1	1
0	1	0	1	1
1	0	0	0	0
1	1	1	0	1

THREE INPUT OR GATE



3 Inputs : A, B, C

$2^3 = 8 \Rightarrow 8$ LINES

(10)

A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

3 Input OR
TRUTH TABLE