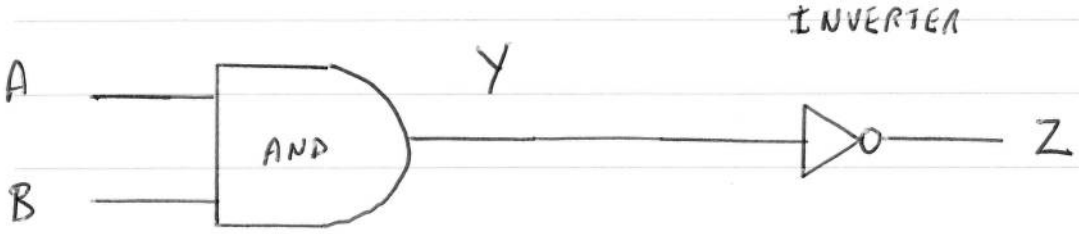
NAND GATE

CONSTRUCTION OF NAND GATE



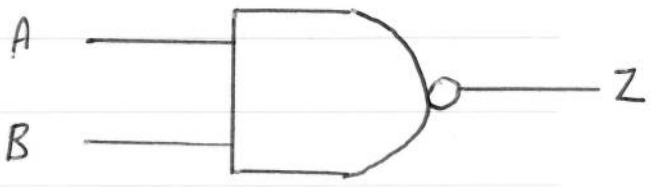
TRUTH TABLE (FOR ABOVE CIRCUIT)

A	B	Y	Z
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

TRUTH TABLE FOR NAND

A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

LOGIC SYMBOL

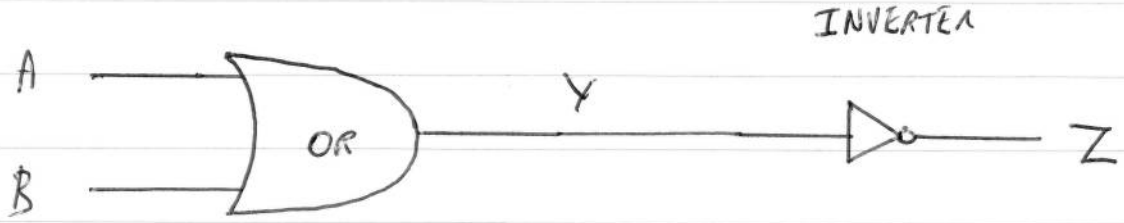


FUNCTIONAL NOTATION

$$Z = \overline{A \cdot B}$$

NOR GATE

CONSTRUCTION OF NOR GATE



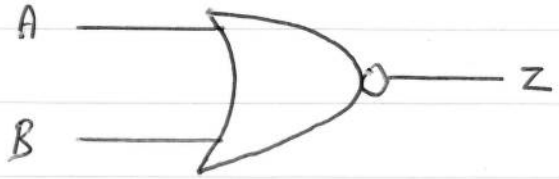
TRUTH TABLE FOR ABOVE CIRCUIT

A	B	Y	Z
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

TRUTH TABLE FOR NOR

A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0

LOGIC SYMBOL

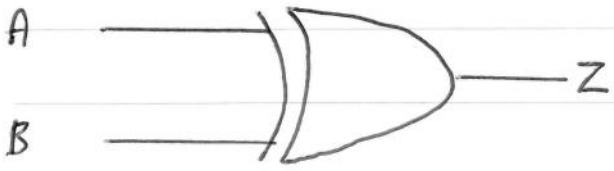


FUNCTIONAL NOTATION

$$Z = \overline{A + B}$$

XOR GATE (EXCLUSIVE OR GATE)

LOGIC SYMBOL



FUNCTIONAL NOTATION

$Z = A \oplus B$

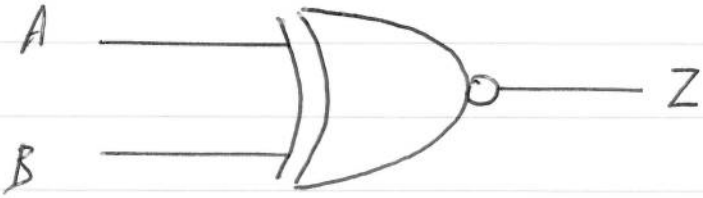
WHEN PRECISELY ONE INPUT IS HIGH (1) THE OUTPUT IS HIGH (1)

TRUTH TABLE FOR XOR

A	B	Z
0	0	0
0	1	1
1	0	1
1	1	0

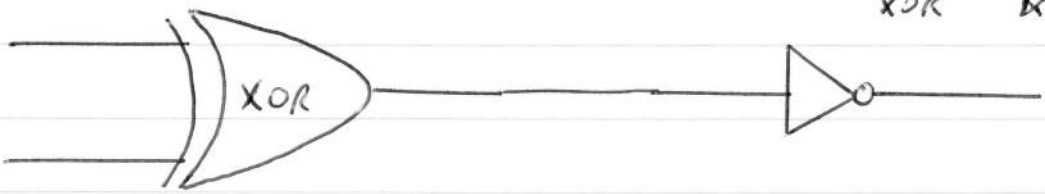
XNOR GATE

ITS FUNCTION IS THE LOGICAL COMPLEMENT OF THE EXCLUSIVE OR (XOR) GATE.



LOGIC SYMBOL

CONSTRUCTION USING XOR & INVERTER



TRUTH TABLE

A	B	Z
0	0	1
0	1	0
1	0	0
1	1	1

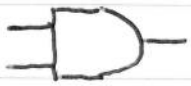
FUNCTIONAL NOTATION

$Z = A \odot B$

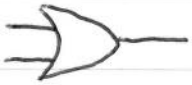
Summary of Gates

		Z					
A	B	AND	OR	XOR	NAND	NOR	XNOR
0	0	0	0	0	1	1	1
0	1	0	1	1	1	0	0
1	0	0	1	1	1	0	0
1	1	1	1	0	0	0	1

AND : $Z = A \cdot B$



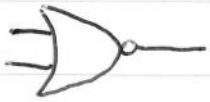
OR : $Z = A + B$



XOR : $Z = A \oplus B$

NAND: $Z = \overline{A \cdot B}$

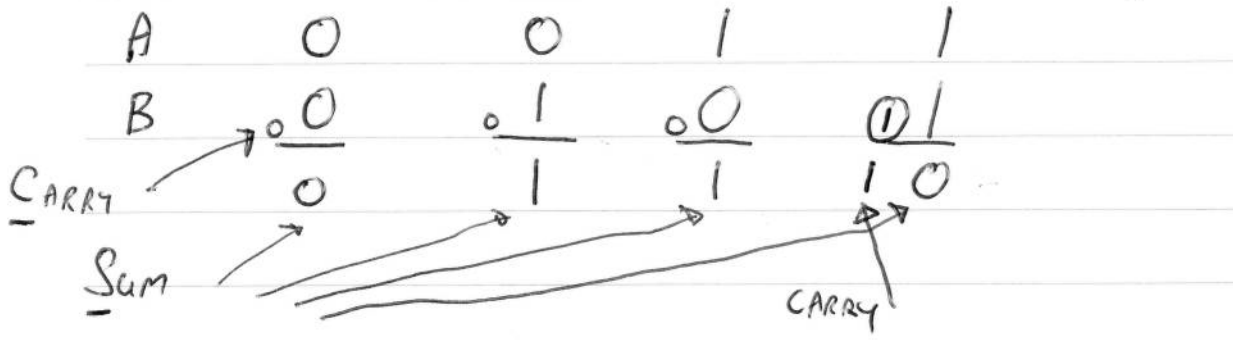
NOR: $Z = \overline{A + B}$



XNOR: $Z = A \odot B$

TRANSISTORS → GATES → CIRCUITS

HALF ADDER CIRCUIT



TRUTH TABLE FOR HALF-ADDER CIRCUIT

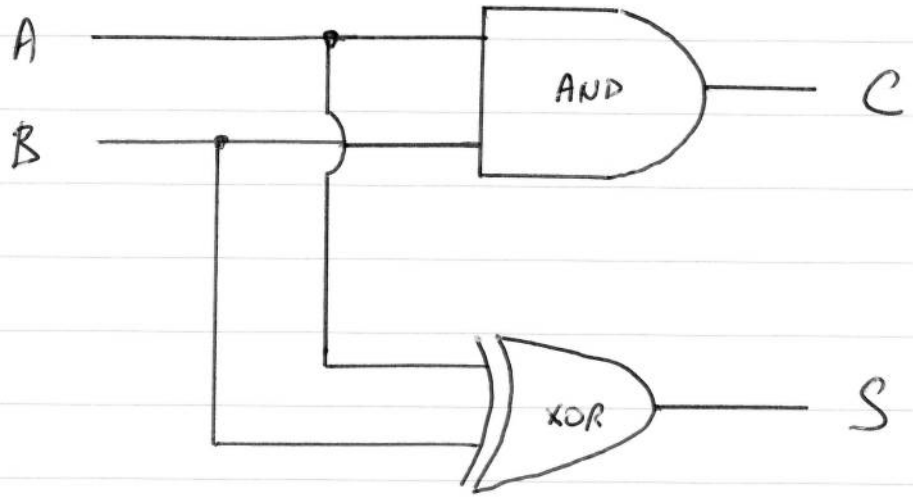
A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

INPUTS OUTPUTS

GATE LEVEL DIAGRAM FOR HALF-ADDER CIRCUIT

$C = A \cdot B$ CARRY IS HIGH WHEN A AND B ARE HIGH

$S = A \oplus B$ XOR FUNCTION

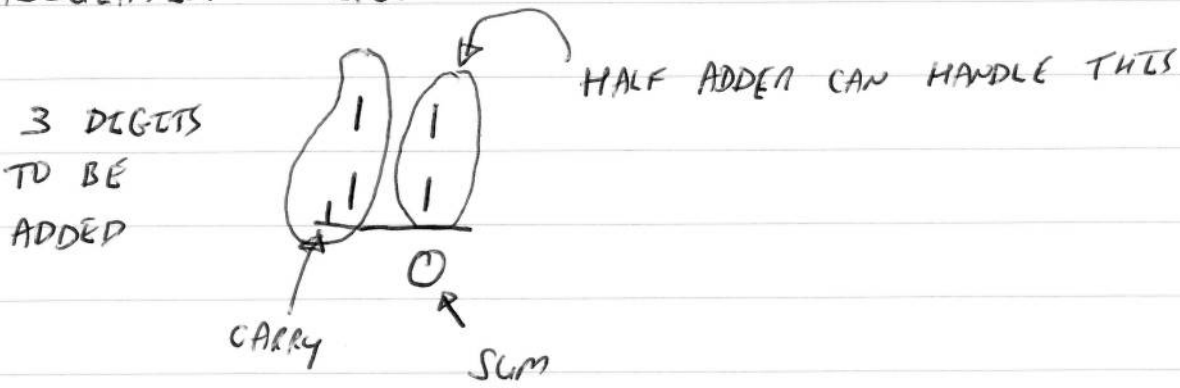


FULL ADDER

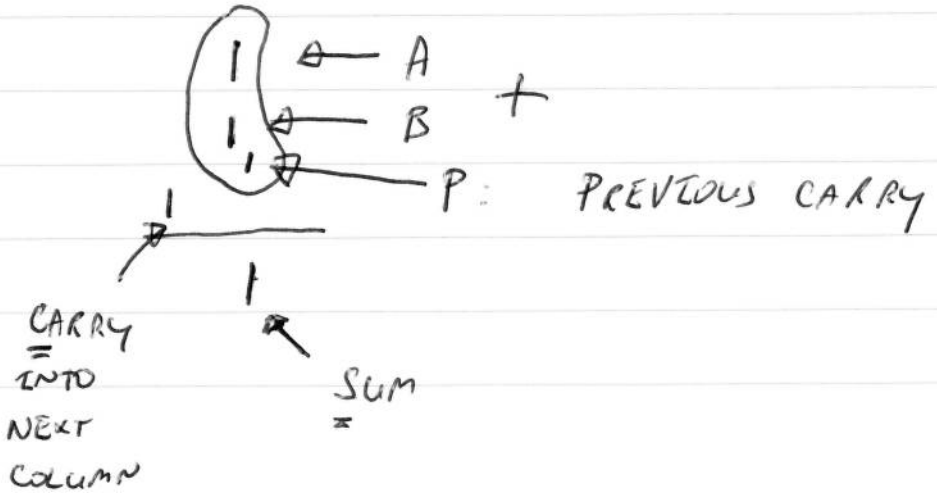
HALF ADDER CAN ADD:

$$\begin{array}{cccc} 0 & 0 & 1 & 1 \\ 0 & 1 & 0 & 1 \end{array}$$

IT CANNOT HANDLE A CARRY FROM A PREVIOUS CALCULATION E.G.



HALF-ADDER HAS ONLY TWO INPUTS A, B.
WE NEED A FULL ADDER TO HANDLE THE ABOVE SCENARIO



FULL ADDER (TRUTH TABLE)

A	B	P	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1