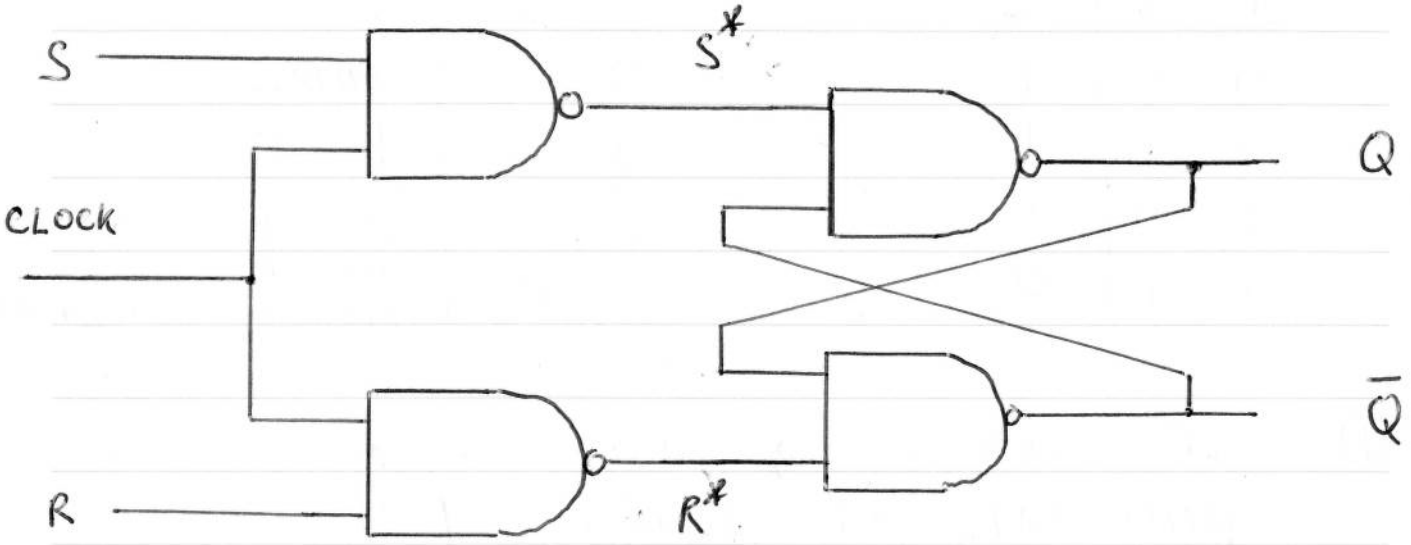
CLOCKED SR FLIP FLOP



TRUTH TABLE FOR CLOCKED SR FLIP FLOP

	CLK	S	R	S^*	R^*	Q	$\bar{Q}$
①	0	X	X	1	1	NO CHANGE MEMORY (LATCHED)	
②	1	0	0	1	1	NO CHANGE MEMORY (LATCHED)	
③	1	0	1	1	0	0	1
④	1	1	0	0	1	1	0
⑤	1	1	1	0	0	INVALID	

METASTABILITY

TABLE 1 | NAND

A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

S-R LATCH (NAND GATES)

$\bar{S}$	$\bar{R}$	Q	$\bar{Q}$
0	0	INVALID	
0	1	1	0
1	0	0	1
1	1	NO CHANGE MEMORY (LATCHED)	

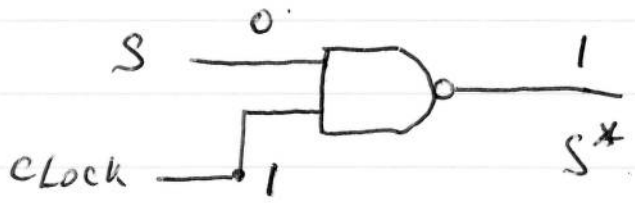
① IF CLOCK IS 0, OUTPUT FROM NAND GATE IS ALWAYS 1 (IRRESPECTIVE OF THE 2ND INPUT)

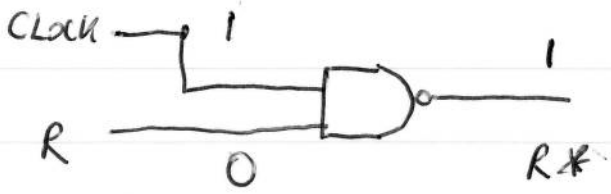
SO OUTPUTS S^* AND R^* WILL BOTH BE 1.

CLK		
A	B	Z
0	0	1
0	1	1

LINE (2)

CLOCK	S	S^*
1	0	1

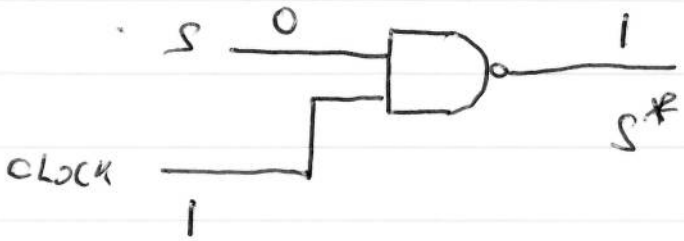


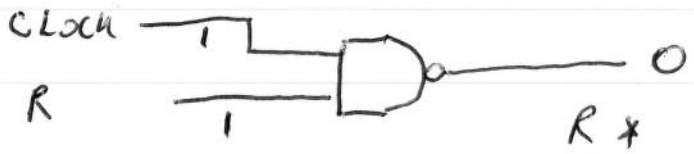


CLOCK	R	R^*
1	0	

LINE (3)

CLOCK	S	R
1	0	1





	CLOCK	R
	1	1

THINK THROUGH LAST TWO LINES, LINES 4 AND 5.