Tues 2nd Dec 2014

UNIVERSAL GATES

DIAGRAMS AB CD EF GH IJ KL MN

NOT AND OR NAND NOR EX-OR EX-NOR

$Z = \overline{A}$ $Z = A \cdot B$ $Z = A + B$ $Z = \overline{A \cdot B}$ $Z = \overline{A + B}$ $Z = A \oplus B$ $Z = \overline{A \oplus B}$

UNIVERSAL GATES

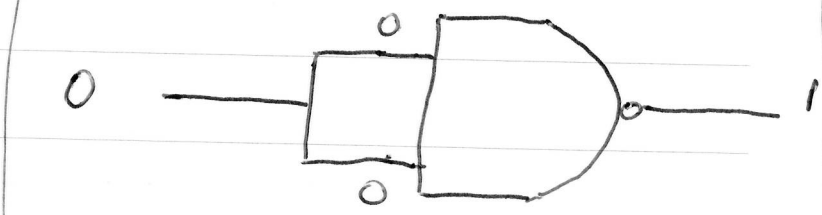
NAND & NOR ARE UNIVERSAL GATES – YOU CAN CONSTRUCT ANY OF THE OTHER GATES USING ONLY NAND GATES OR USING ONLY NOR GATES

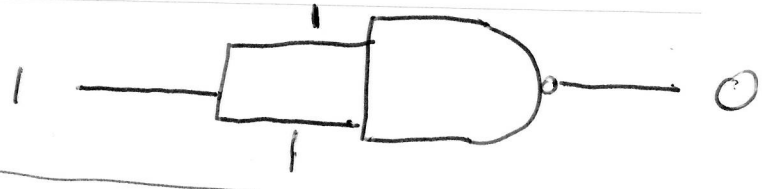
(INVERTER)
NOT

NAND

NAND		
A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

A. NOT (INVERTER USING NAND)



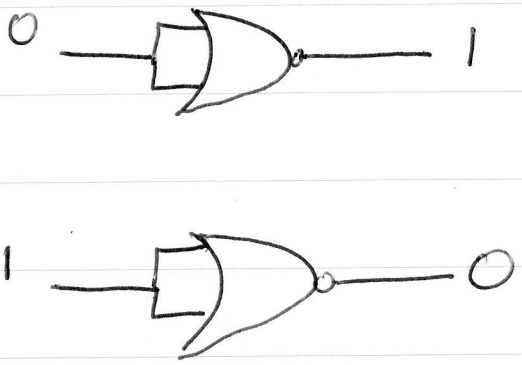


(INVERTER)
NOT

NOR

NOR

A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0



B INVERTER USING NOR GATE

AND

NAND

NAND INVERTER

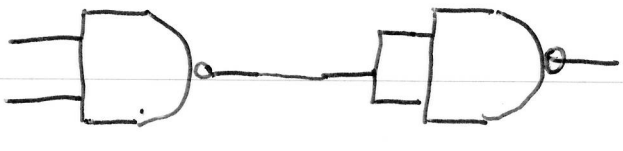
FUNCTIONALITY

NAND

A	B	Z	INPUT
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

AND

≡ AND USING ONLY NAND



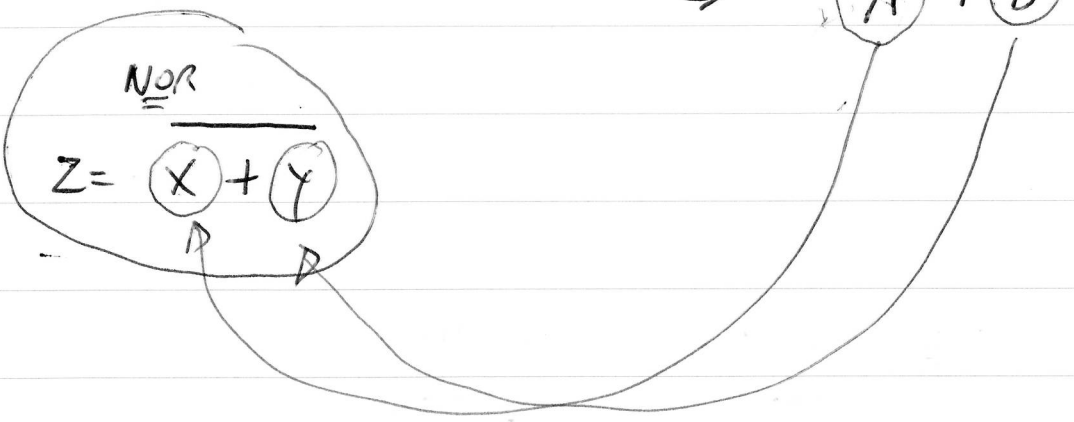
ACTING AS INVERTER

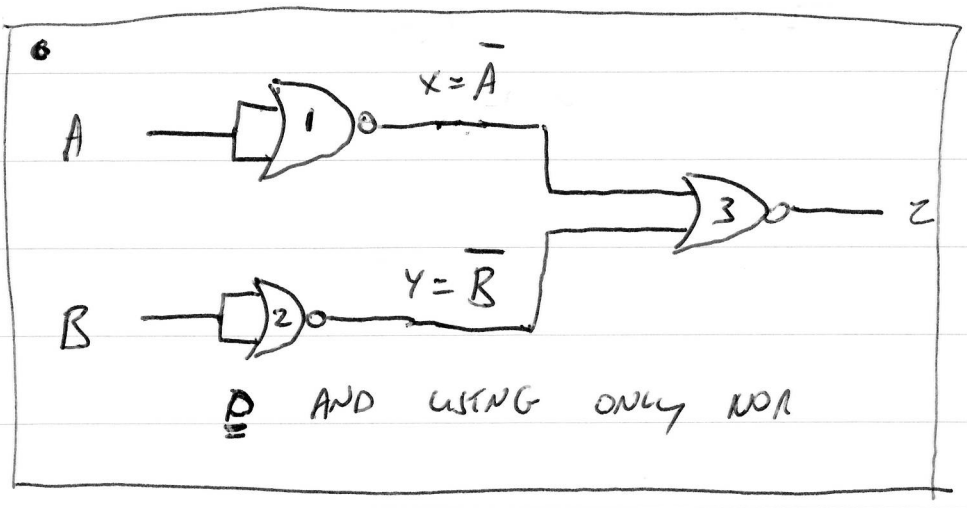
AND ⟶ USING NOR

AND

$A \cdot B \Rightarrow \bar{\bar{A}} \cdot \bar{\bar{B}}$

$\Rightarrow \overline{\bar{A} + \bar{B}}$





AND USING ONLY NOR

(5)

OR

0
1
1
1

NOR

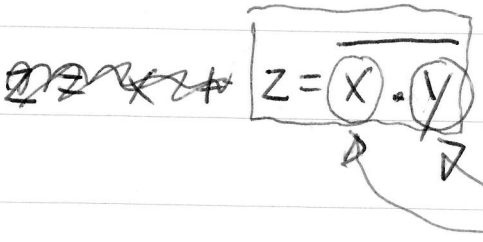
A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0

PERFECT INDUCTION

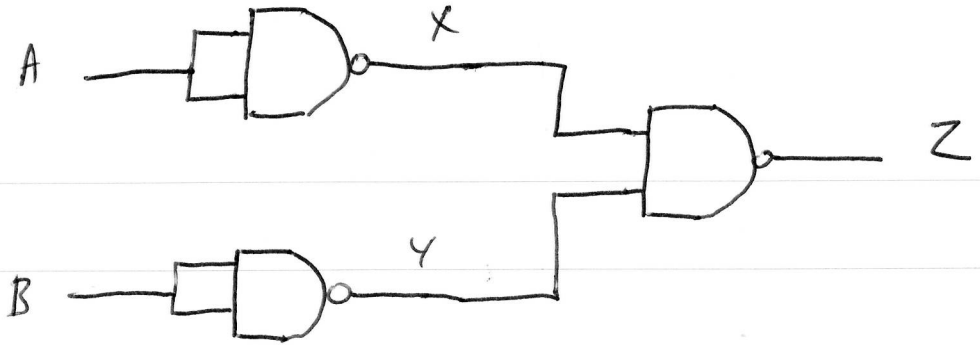
A	B	X	Y	Z
0	0	1	1	0
0	1	1	0	0
1	0	0	1	0
1	1	0	0	1

* OR USING NAND.

NAND



E OR USING ONLY NAND



A	B	X	Y	Z
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

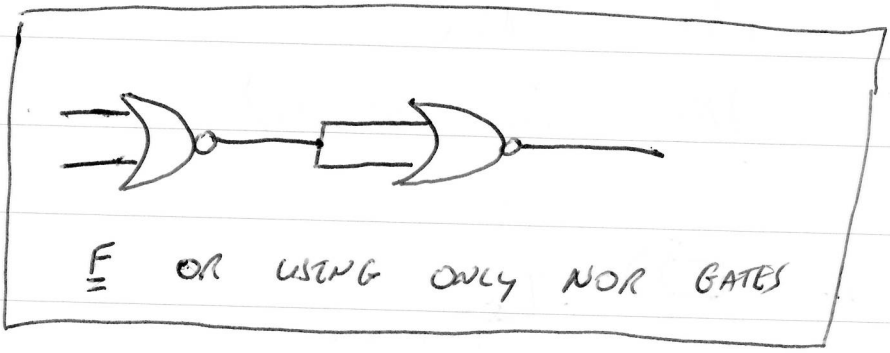
OR

(7)

OR USING NOR

HINT

NOR

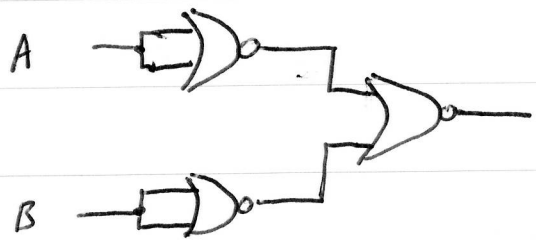


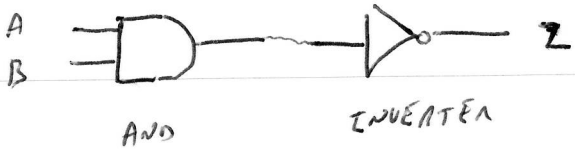
F OR USING ONLY NOR GATES

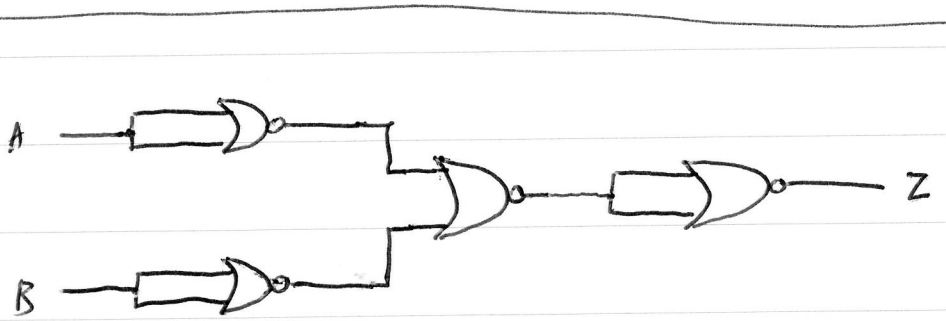
G NAND USING NAND

NAND USING ONLY NOR GATES

HINT: This is NOR representation of AND. (SEEN ON P.4)





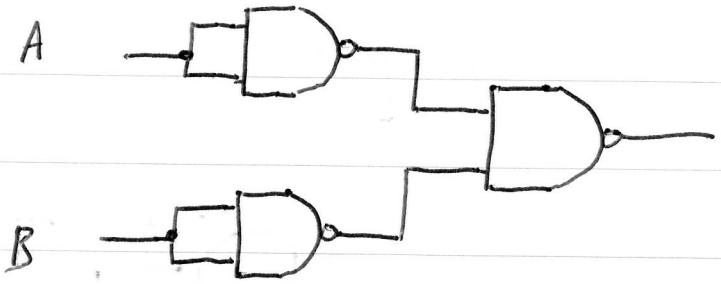


H NAND USING ONLY NOR

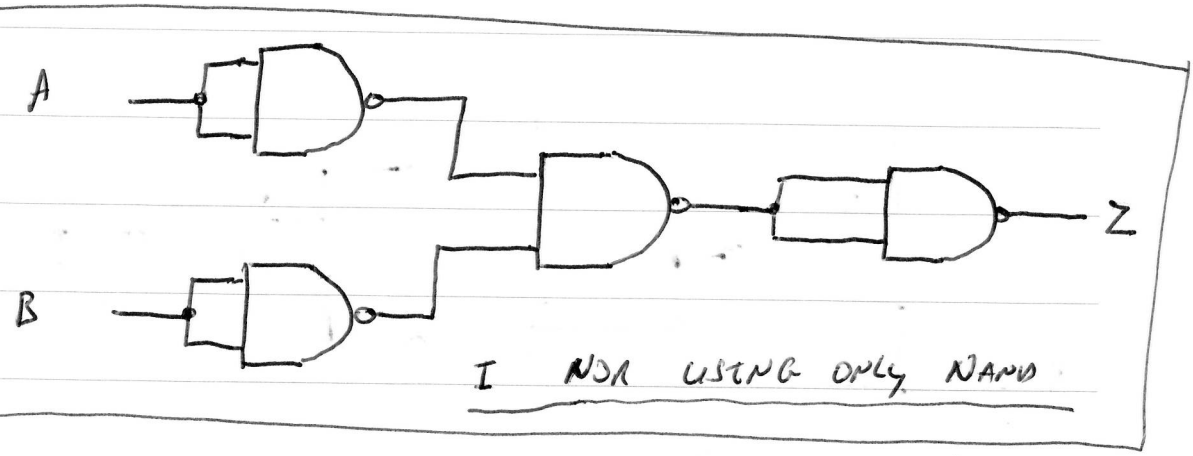
NOR GATE USING ONLY NAND

HINT:

This is ~~OR~~ NAND REPRESENTATION OF OR (SEEN ON P.6)

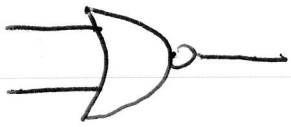


OR INVERTER } NOR FUNCT.

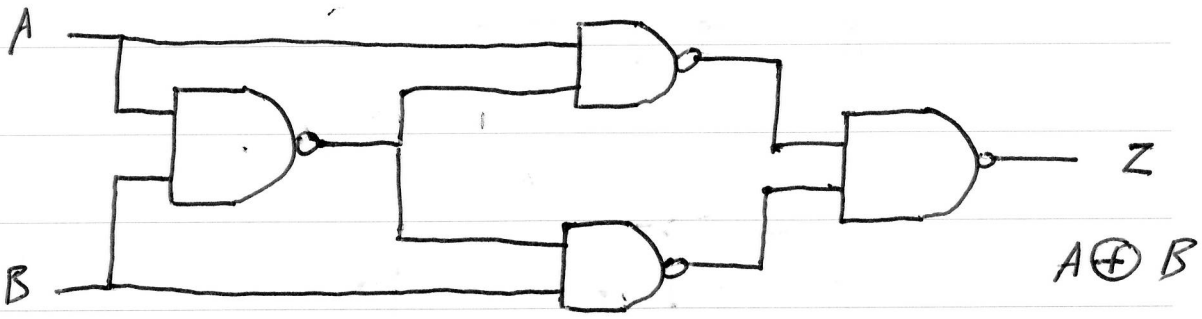


I NOR USING ONLY NAND

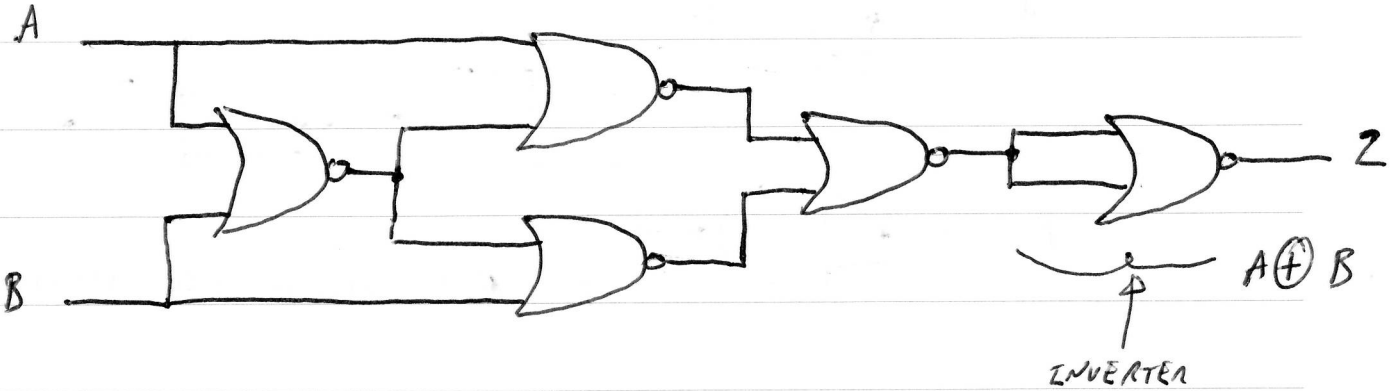
J NOR GATE USING ONLY NOR



K XOR USING ONLY NAND



L XOR USING ONLY NOR



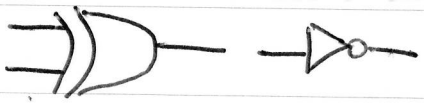
EXNOR

EXNOR

A	B	Z
0	0	1
0	1	0
1	0	0
1	1	1

XOR

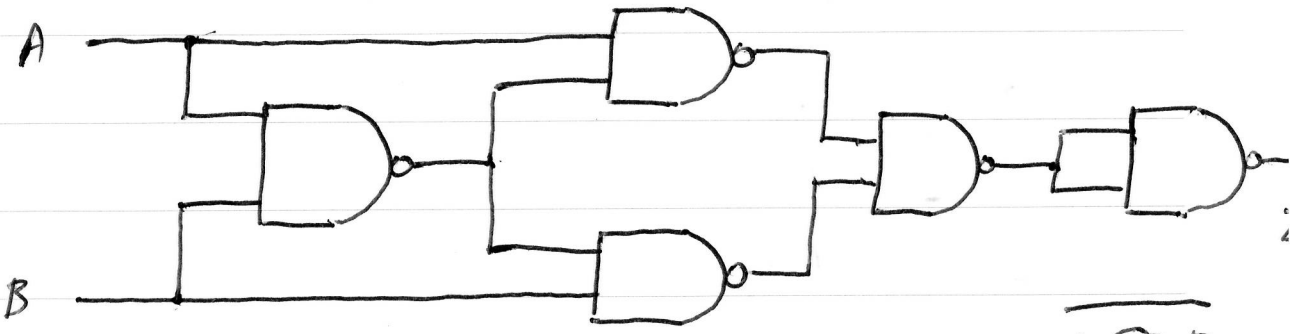
A	B	Z
0	0	0
0	1	1
1	0	1
1	1	0



~~XOR~~ EXNOR (USING ONLY NAND)

- TAKE XOR (PRODUCED USING NAND GATES)
- ADD AN INVERTER
- JOB DONE

EXNOR USING ONLY NAND

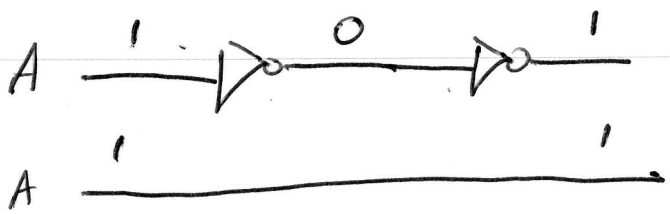


$Z = \overline{A \oplus B}$

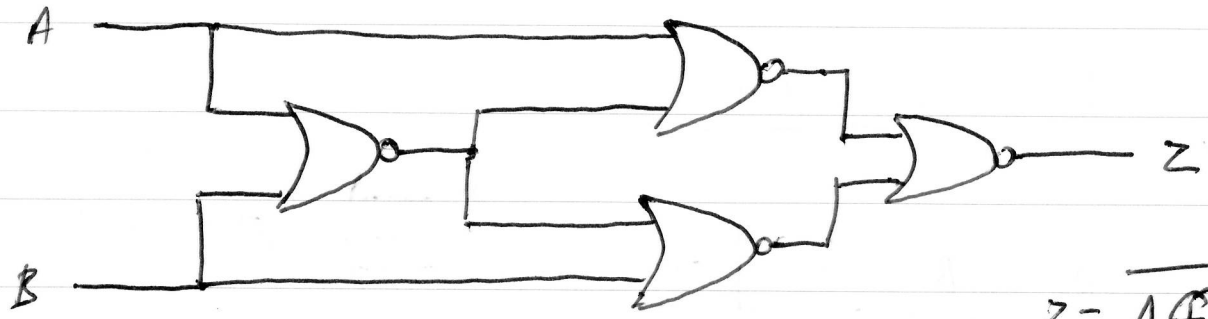
EXOR USING ONLY NOR

WE COULD TAKE XOR (PRODUCED USING NOR GATES) ON P. 10
AND ADD ON AN INVERTER.

BUT, ~~IF~~ ~~IT~~ IT ALREADY HAS AN INVERTER AT THE END, (SO SIMPLY DROP OFF THE INVERTER AT THE END)



N EXNOR USING ONLY NOR GATES

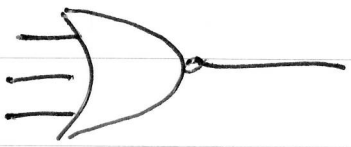


$Z = \overline{A \oplus B}$

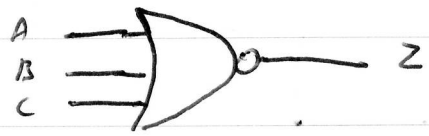
APOLLO SCHEMATICS — BUILT USING "NOR" GATES

3 INPUT OR:

A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1



3 INPUT NOR



A	B	C	Z
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

FOR APOLLO SCHEMATICS, SEE

http://klabs.org/history/ech/agc_schematics

ALSO Look for Apollo-Guidance-Computer-2009.pdf